PAPER

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Self-aligned photolithography for the fabrication of fully transparent high-voltage devices

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Abstract

High-voltage devices, working in the range of hundreds of volts, are indispensable elements in the driving or readout circuits for various kinds of displays, integrated microelectromechanical systems and x-ray imaging sensors. However, the device performances are found hardly uniform or repeatable due to the misalignment issue, which are extremely common for offset drain high-voltage devices. To resolve this issue, this article reports a set of self-aligned photolithography technology for the fabrication of high-voltage devices. High-performance fully-transparent high-voltage thin film transistors, diodes and logic inverters are successfully fabricated with this technology. Unlike other self-aligned routes, opaque masks are introduced on the backside of the transparent substrate to facilitate proximity exposure method. The photolithography process is simulated and analyzed with technology computer aided design simulation to explain the working principle of the proximity exposure method. The substrate thickness is found to be vital for the implementation of this technology based on both simulation and experimental results. The electrical performance of high-voltage devices is dependent on the offset length, which can be delicately modulated by changing the exposure dose. The presented self-aligned photolithography technology is proved to be feasible in high-voltage circuits, demonstrating its huge potential in practical industrial applications.

Keywords: high-voltage, self-aligned, thin film transistors, diodes, inverters, transparent

Supplementary material for this article is available online

(Some figures may appear in colour only in the online journal)

1. Introduction

High-voltage thin-film transistors (HVTFTs) and high-voltage diodes (HVDs) are indispensable elements in the driving circuits of various displays, including ferroelectric liquid crystals displays [1], electrophoretic displays [2], electro-optical displays [3], field emission displays [4] and braille displays [5, 6], as well as in the readout circuits of x-ray imaging sensors [7]. Recently, potential applications of HVTFTs and HVDs in energy management for energy harvesting systems were demonstrated in building integrated photovoltaics (BIPVs) [8] and triboelectric nanogenerators (TENGs) [9], respectively. To avoid breakdown occurrence in these crucial HV devices, the electric potential need to descend across a sufficient length along either vertical or horizontal directions. In the vertical case, thick insulator layers are employed to sustain high voltage drop in HVTFTs [10, 11] and HVDs [12]; while in the horizontal situation, offset regions are introduced [5, 13–18]. The offset solution is superior to the thick gate dielectric alternative, in virtue of its larger gate capacitance

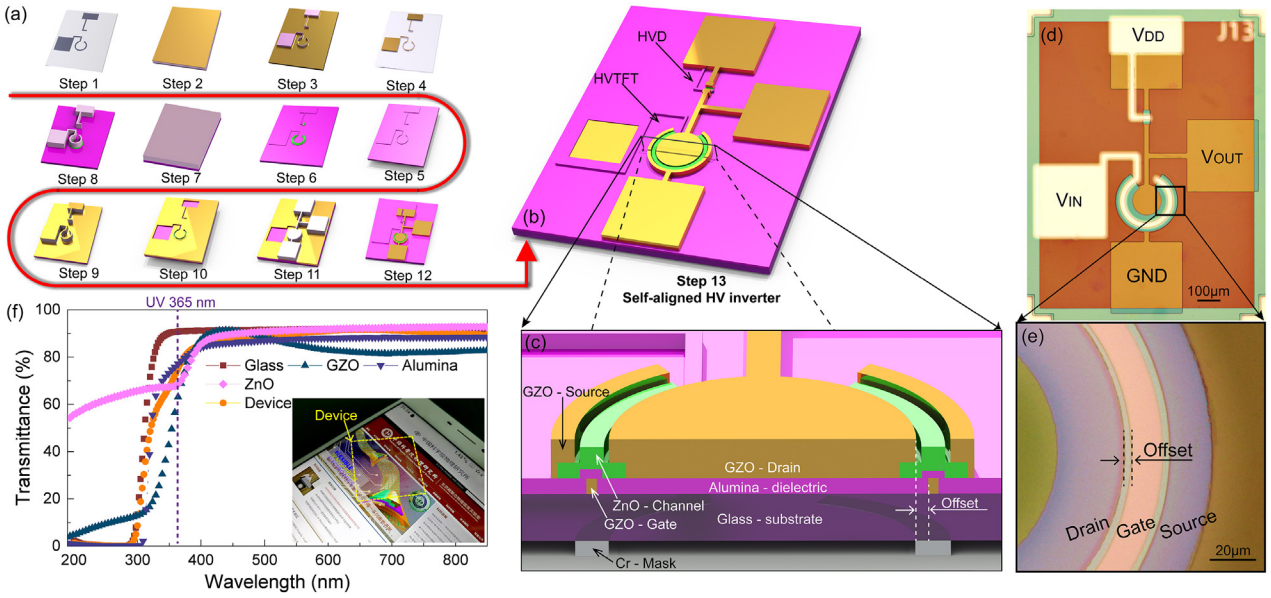

Figure 1. (a) A typical fabrication procedure of self-aligned HV inverters. (b) Structure diagram of a completed self-aligned HV inverter, which contains an HVTFT drive and an HVD load. (c) Cross-sectional view of an HVTFT. (d) Optical microscope image of a self-aligned HV inverter. (e) Local enlarged image of an HVTFT which shows the offset region between gate and drain. (f) Optical transmittance spectra of a completed 25 × 25 mm^2 wafer and all the transparent materials involved in the fabrication. The inset is the photograph of the fully-transparent device on the screen of a phone.

and thus better gate control capability. As a critical device parameter, the offset length determines the magnitude of the on-state current (I_{ON}) and breakdown voltage (V_{BR}). In most cases, an increase of the offset length will lead to the increase of V_{BR} and decease of I_{ON}, and vice versa [5, 9, 14, 15, 19]. However, it is hard to precisely control the offset length, due to the significant misalignment issue [19–22] during the patterning of drain and gate electrodes. That will result in a poor uniformity and repeatability of the device performance in offset drain HVTFTs and HVDs.

This work presents a kind of self-aligned photolithography technology for the fabrication of offset drain high-voltage devices, aiming to solve the misalignment issue. High-performance fully-transparent HVTFTs, HVDs and HV inverters are successfully fabricated using this method. Besides regular current–voltage (*I*–*V*) tests, the uniformity of the self-aligned HVTFTs is also examined. The principle of the self-aligned photolithography is studied with optical simulation. Furthermore, by modulating the exposure dose, the offset length, and thus the device performance, can be precisely controlled. Finally, HV inverters with an HVTFT drive and an on-chip HVD load are constructed and evaluated, demonstrating the feasibility of the presented technology in high-voltage circuits.

2. Experiments

2.1. Device fabrication

The fabrication procedure of the self-aligned photolithography process is illustrated in figure 1(a). Step 1: chromium (Cr, 50 nm thick) pattern was deposited onto the backside of a glass substrate (170 μm thick). Step 2: gallium zinc oxide (GZO, 100 nm thick) gate electrode layer was deposited onto the front of the substrate. Step 3: AZ6130 positive photoresist pattern was formed after exposure from the backside direction using the Cr pattern as mask (UV 365 nm, dose = 120 mJ cm^{-2}). Step 4: the gate electrode was formed after wet etching of GZO using photoresist as the mask. Step 5: the alumina (Al_2O_3, 100 nm thick) dielectric layer was deposited via atomic layer deposition (ALD) at 100 °C with trimethylaluminum (TMA) and water as precursors. Step 6: the zinc oxide (ZnO, 40 nm thick) channel layer was deposited via radio frequency magnetron sputtering (rf-MS) at room temperature in Ar/O_2 mixed atmosphere with a power of 70 W (2 inch target) and pressure of 0.4 Pa and patterned by photolithography and wet etching in 1% HCl for 3 s. Step 7: the same AZ6130 photoresist was coated. Step 8: the photoresist pattern was formed after exposure from the backside direction with a smaller dose of 90 mJ cm^{-2} and development. Step 9: the GZO (100 nm thick) source/drain electrode layer was deposited onto the front side. Step 10: photoresist and the GZO on it was removed after lift-off. Step 11: the same AZ6130 photoresist was coated and patterned by photolithography. Step 12: wet etching of GZO and stripping of photoresist. Step 13: self-aligned inverter was completed after opening the contact via-hole and shorting the gate and drain of the HVD. The fabrication process was also depicted in detail with the micro-photographs and optical simulation in supporting information (stacks.iop.org/JPhysD/51/175102/mmedia) S1 and S2, respectively. Note that special attention should be taken to avoid contamination or scratching of Cr mask during the fabrication. Upon completing the fabrication, the devices were then post-annealed at 300 °C in air for 1 h.

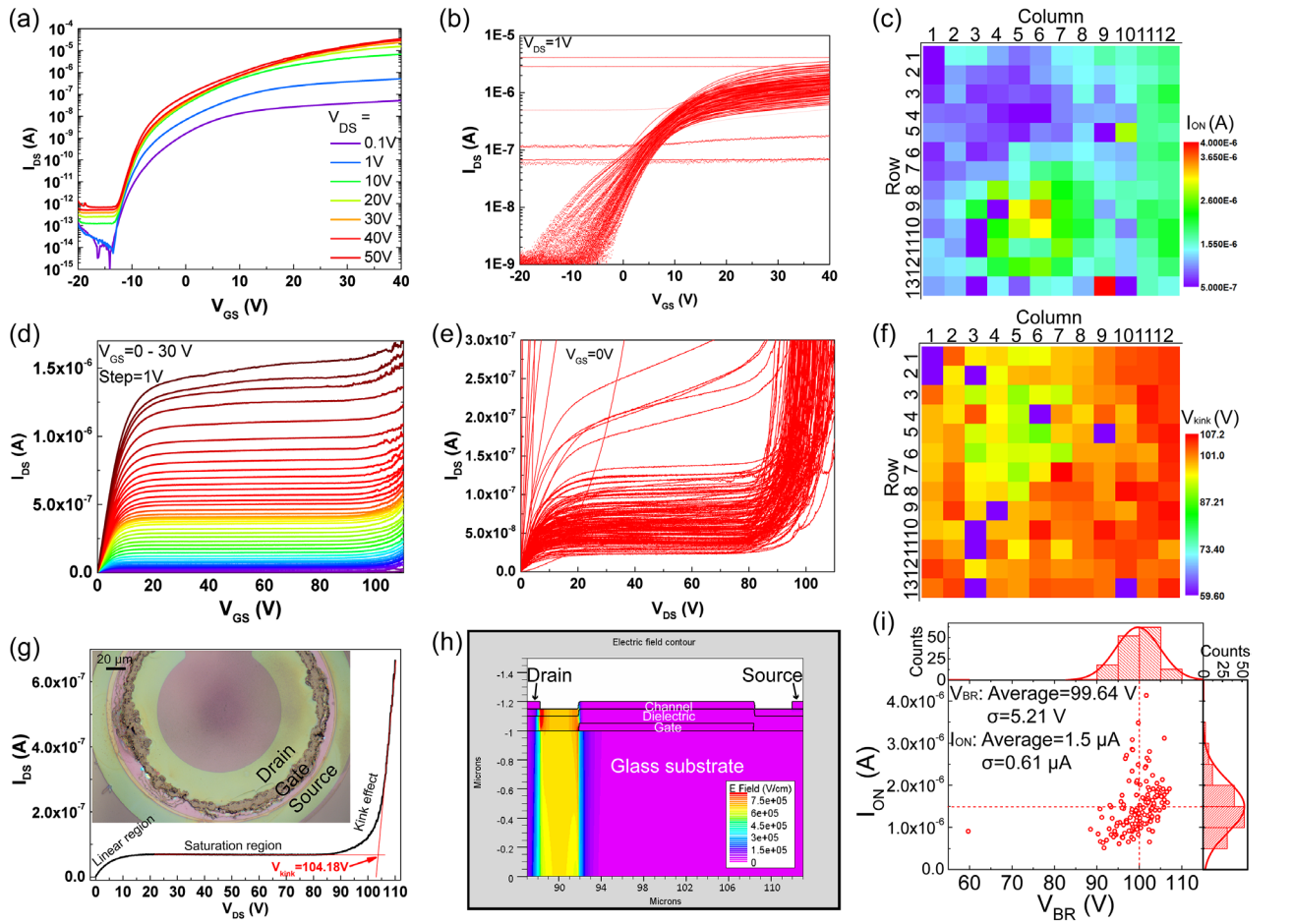

Figure 2. (a) Transfer characteristics of an HVTFT with on/off ratio over 10^7 and ultra-low off-state current below 10^{-15} A μm^{-1}. (b) Summary of transfer curves of 156 HVTFTs on one wafer. (c) Wafer map of on-state current over a 25 × 25 mm^2 glass substrate. (d) Output characteristics of an HVTFT indicating its capability of regulating current at high voltage. (e) Summary of output curves of the 156 HVTFTs. (f) Wafer map of kink voltage. (g) One output curve with $V_{GS} = 0$, in which there are linear, saturation and kink effect regions. Inset shows the microscope image of a burned-out device, with the burned region locating between the drain and gate. (h) TCAD simulation of the electric field strength, indicating that the weak points located near the gate and drain electrodes edges. (i) Statistics of on-state current and kink voltage values from 156 devices. The uniformity is improved with the presented self-aligned photolithography technology.

2.2. Device characterization

I–V characteristics measurements in figures 2(a), 4(c) and 5(b) are performed in a dark air at room temperature using source-measurement unit included in Keithley 4200 semiconductor characterization system. Other *I–V* characteristics of the HVTFTs and the voltage-transfer characteristics of the HV inverters are performed by a self-assembled *I–V* test system with a Keithley 6487 picoammeter and two Keithley 2400 source meters. The transient response measurement in figure S3 is performed with a square wave generated by a Keithley 3390 function generator and recorded by a Tektronix TDS1000B-SC oscilloscope via P2220 passive voltage probes (resistance = 10 MΩ). The transmittance spectra in this report are obtained with a SHIMADZU UV 3600 plus spectrophotometer.

2.3. TCAD simulation

The process simulations are performed by ATHENA_Optlith simulator included in the Silvaco TCAD software. The mask in the simulation shares the same size with that in the experiments. The exposure light is i line of mercury lamp (UV 365 nm). The electric field simulations are performed by ATLAS simulator. A nonlinear mesh was defined to accurately characterize the parameters in active areas while coarsely elsewhere. On this basis, a ZnO layer (40 nm thick, energy gap $E_g = 3.37$ eV, affinity $\chi = 4.5$ eV) and an Al_2O_3 layer (100 nm thick, dielectric constant $\varepsilon_r = 9.3$) were defined to serve as the channel and dielectric layers, respectively, with the conductor (work function $\Phi_M = 4.33$ eV) serving as contact electrodes. Fermi–Dirac statistics model was used to get a precise description of electrons in thermal equilibrium.

3. Results and discussion

3.1. Device structure

After the self-aligned photolithography process (figure 1(a)), the HV inverter is constructed with an HVTFT drive and an HVD load as shown in figure 1(b). The cross-sectional view (figure 1(c)) shows the structure diagram of the HVTFT, in

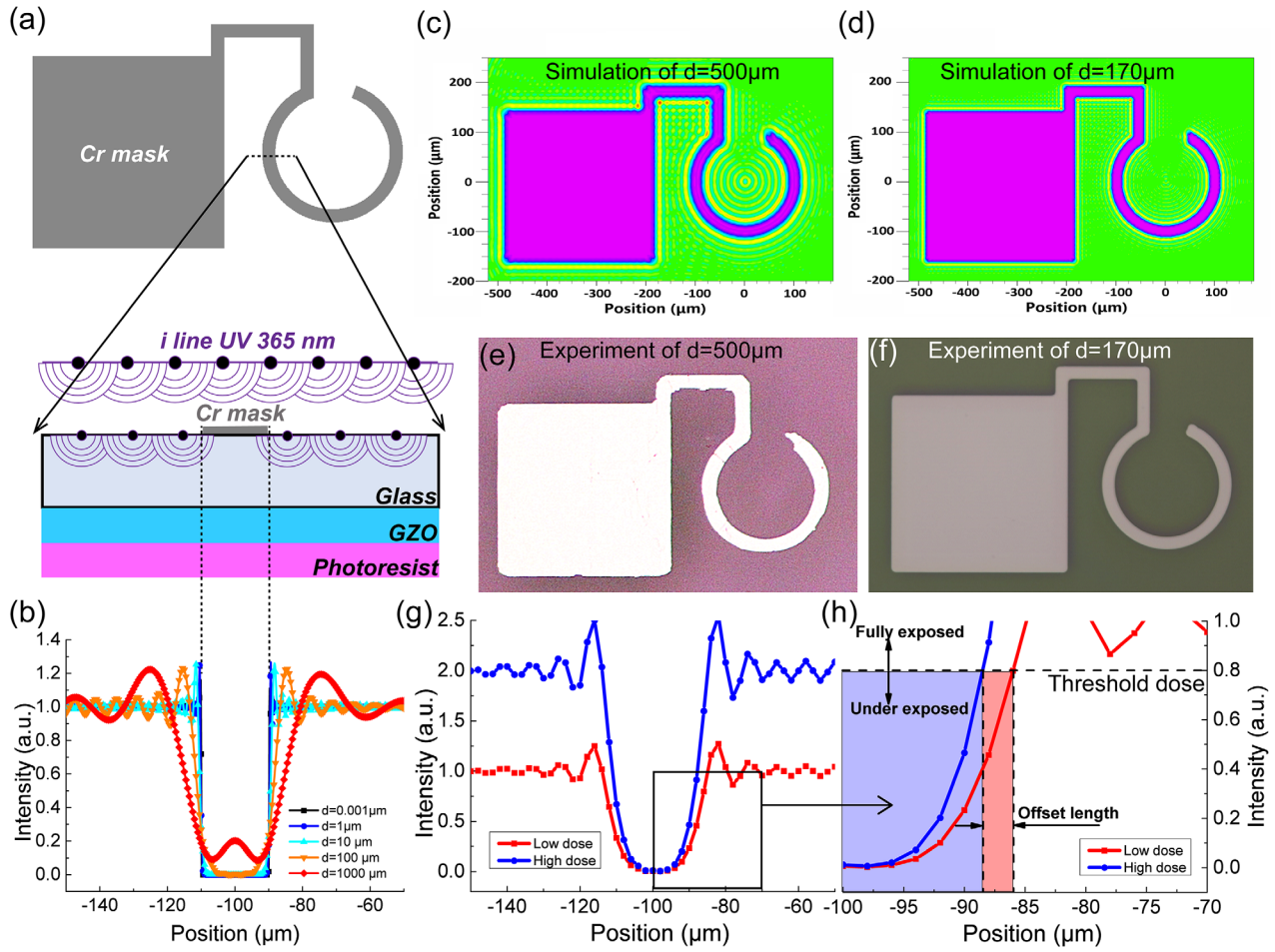

Figure 3. (a) The proximity exposure method with Cr mask on the backside of the glass substrate. (b) The penumbral region increases with the distance between the mask and photoresist. TCAD simulation of normalized exposure intensity with 500 μm-thick (c) and 170 μm-thick (d) glass substrates. Self-aligned photolithography experiments with 500 μm-thick (e) and 170 μm-thick (f) glass substrates. Both the simulations and experiments indicate that 170 μm is better than 500 μm. (g) Exposure intensity with high and low exposure doses. (h) The penumbral regions of high and low dose exposure intersect with the threshold dose, and the distance between the two intersection points gives the offset length.

which the channel length is almost the same as the Cr mask, while the gate length is shorter due to the overexposure in step 3. The length distance between the gate and the drain forms an offset region, which is of particular importance to the device performance. Figure 1(d) shows an optical microscope picture of one completed HV inverter. Figure 1(e) shows a local enlarged picture of the HVTFT, in which the offset length is approximately 2 μm. Finally, after removal of the Cr mask with ammonium ceric nitrate [$(NH_4)_2Ce(NO_3)_6$] solution, the device becomes fully-transparent in visible spectrum range with a high transmittance over 80% (figure 1(f)).

3.2. Electrical performance uniformity

Figure 2(a) shows the transfer curves of an HVTFT (2 μm offset) with a high on/off ratio over 10^7 as well as a low off-state current (I_{OFF}) below 10^{-15} A μm^{-1}, which guarantees ultra-low standby power dissipation in various applications [23]. The transfer curves of a total of 156 devices on one wafer are summarized in figure 2(b). Figure 2(c) shows the wafer map of I_{ON} over a 25 $\times$ 25 mm^2 glass substrate with an average value of 1.5 μA and standard deviation (σ) of 0.61 μA (figure 2(i)). Figure 2(d) shows the output curves with maximum V_{DS} of 110 V and V_{GS} from 0 to 30 V in 1 V step, indicating the capability of regulating current at high voltage. Unlike the conventional low-voltage TFTs [24, 25], the output curve has three distinguishable regions: the linear, saturation and kink-effect regions (figure 2(g)). At V_{DS} lower than 90 V, the HVTFT goes through the linear region and then the saturation region as conventional TFTs, while at V_{DS} higher than 90 V, kink effect occurs and I_{DS} starts to increase exponentially with V_{DS}. Further increase of V_{DS} leads to a combined effect of kink effect and self-heating [15, 26], which ultimately leads to the breakdown of device as shown in the inset of figure 2(g). Technology computer aided design (TCAD) simulation of the electric field strength shows that the weak points locate near the gate and drain edges (figure 2(h)), which agrees well with the burned-out device in the inset of figure 2(g) and other reports [8, 9, 15, 16]. The output curves of the 156 devices are summarized in figure 2(e). Figure 2(f) shows the wafer map of kink voltage (V_{kink}) values for these HVTFTs, with an average V_{kink} of 99.64 V and σ of 5.21 V (figure 2(i)). The σ of I_{ON} and V_{kink} in these HVTFTs is

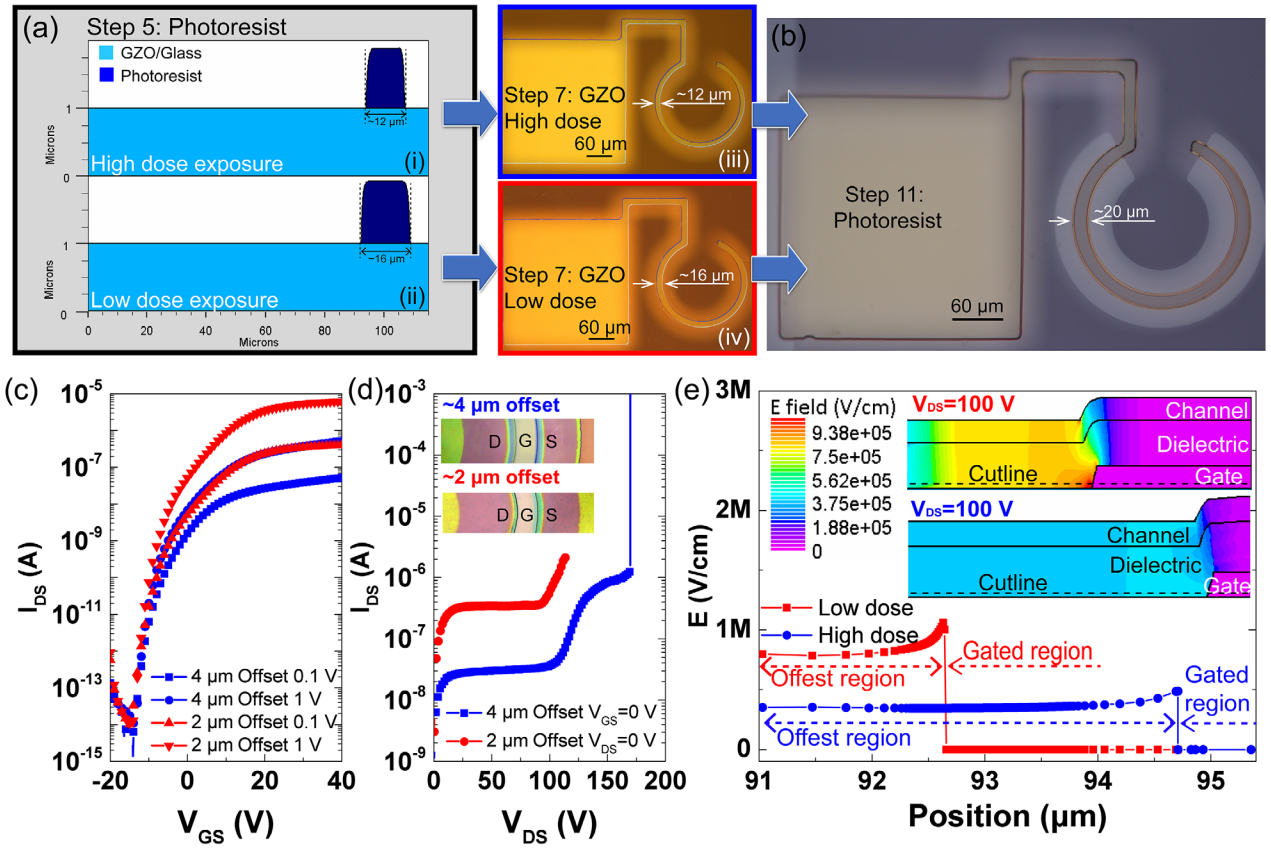

Figure 4. (a) TCAD simulation of the fabrication process in step 3 with high (i) and low (ii) dose exposure. The high dose exposure narrows the photoresist by widening the fully exposed area. The photoresist is used as the mask in subsequent etching, forming GZO gate with short (iii) and long (iv) lengths. (b) Microscope image of HVTFT in step 8. (c) Transfer curves of HVTFTs with 2 μm and 4 μm offset lengths, respectively, in which the on-state current of the former is one order higher than the latter. (d) Output curves of HVTFTs with 2 μm and 4 μm offset lengths, respectively, in which the kink voltage of the former is 20 V smaller than the latter. (e) TCAD simulation of the electric field strength along the cutline near the channel dielectric interface. The 4 μm offset device has much smaller electric field than the 2 μm one.

much smaller than those in our previous report [9], indicating that the self-aligned photolithography technology can improve the uniformity of the high-voltage devices.

3.3. Self-aligned photolithography

The principle of the self-aligned photolithography is presented in figure 3. Distinguished from conventional self-aligned photolithography technologies which utilized the opaque gate on the front side of the transparent substrate as the mask in the backside exposure process [27, 28], the opaque Cr mask is introduced onto the backside of the glass substrate to facilitate the proximity exposure method [29–31] as shown in figure 3(a). In the proximity exposure method, there is a penumbral region with the length $\delta = k(\lambda d)^{1/2}$ [32], where k is a process-related parameter, the typical value of which is around 1, λ the wavelength of the exposure light and d the distance between mask and the photoresist, i.e. the glass thickness in this case. Figure 3(b) shows the simulated light intensity profile through the Cr mask with various glass thickness. The penumbral region length increases monotonously with the glass thickness, theoretically $\delta \approx 0.02$ μm, 0.60 μm, 1.91 μm, 6.04 μm and 19.10 μm for $d = 0.001$ μm, 1 μm, 10 μm, 100 μm and 1000 μm. Two kinds of glasses with a thickness of 500 μm and 170 μm were employed in the simulations and experiments to verify the influence of the substrate thickness on the proximity exposure process. There are profounder fluctuations, corresponding to larger penumbral region, in the thicker substrate (figure 3(c)) than in the thinner one (figure 3(d)). Accordingly, a higher pattern accuracy will be achieved in the case of the thinner substrate (figure 3(f)) compared with the thicker one (figure 3(e)). Since 170 μm is thinner than the commonly used 0.5 mm–0.7 mm in industrial production lines, a small-area wafer was more preferred in the self-aligned technology to avoid the fragmentation issue. On the base of a 170 μm thick glass substrate, high and low dose exposures were simulated (figure 3(g)). Obviously, intensity in the high dose case changes faster than that in the low dose case. Supposing the threshold of the exposure intensity is 0.8 (the minimum intensity of fully exposure), the width of the underexposed photoresist, which remains after development, would differ by 2 $\times$ offset length in the two cases (figure 3(h)). The presented self-aligned photolithography technology employs two times of backside exposure process, the first for the gate etching (step 3) and the second for the source drain lift-off (step 8). By modulating the exposure dose in the two exposure processes, the offset region with desired length between the gate and drain could be achieved as expected.

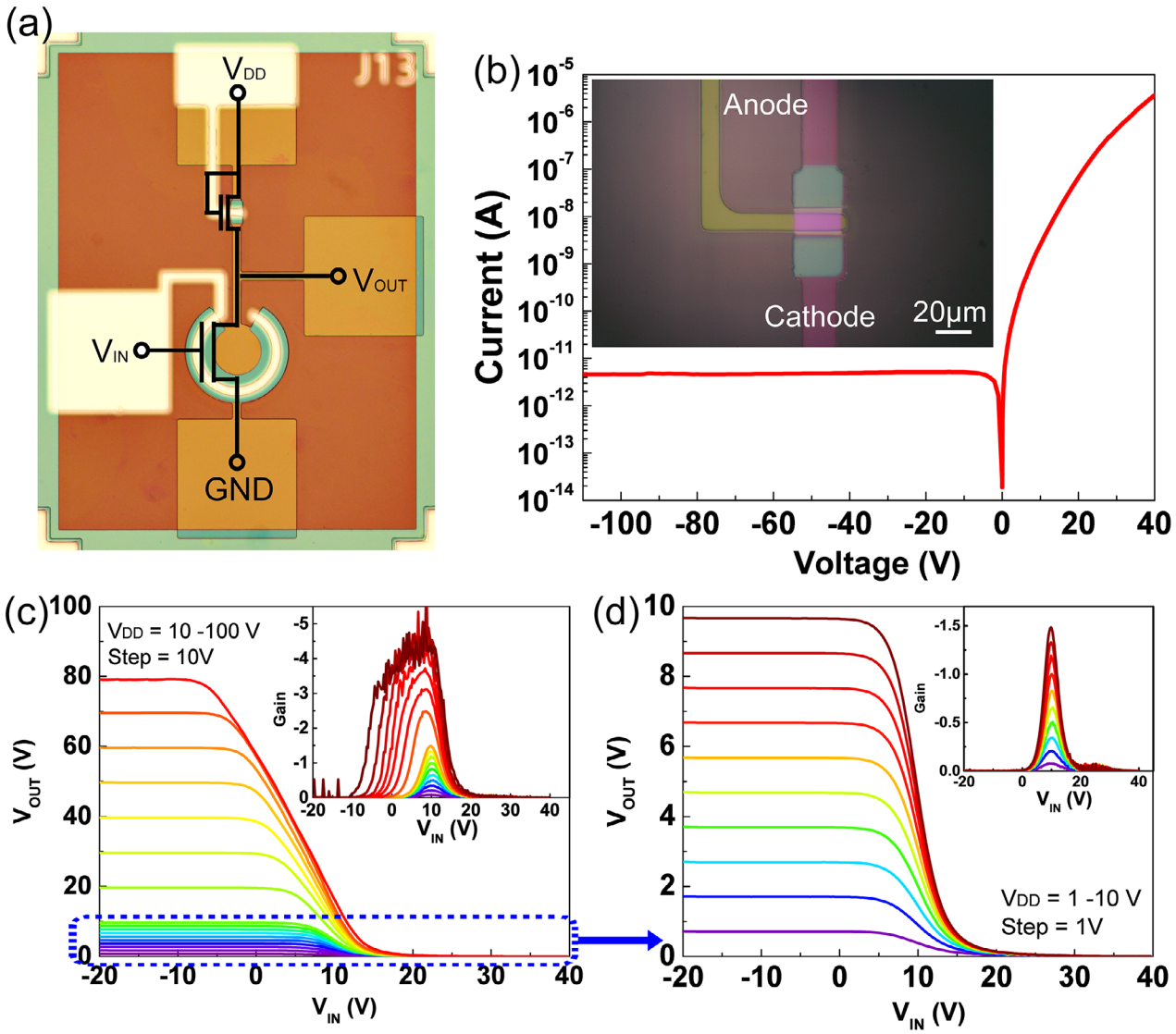

Figure 5. (a) Structure diagram of an HV inverter which is composed of an HVTFT drive and an HVD load. (b) *I–V* characteristics of HVD with rectification ratio of ~10^6 and V_{BR} more than 110 V. (c) Voltage-transfer characteristics of the HV inverter with a maximum operation voltage of 80 V. Inset is the voltage gain. (d) Low-voltage operation of the HV inverter down to 1 V. Inset is the voltage gain.

3.4. Modulation of offset length

Furthermore, the offset length could be modulated through changing the backside exposure dose in step 3. According to the analysis in figures 3(g) and (h), higher dose widens the fully exposed area, and thus leading to narrower photoresist after development as shown in the simulation (figure 4(a)(i) and (ii)). Subsequently, etching and stripping (step 4) were conducted to form GZO gates with length of approximately 12 (figure 4(a)(iii)) and 16 μm (figure 4(a)(iv)). After the second self-aligned photolithography in step 8, the photoresist pattern with the feature length of 20 μm was formed (figure 4(b)), which defines the channel length of the HVTFT. After completing the following steps, the self-aligned HVTFTs with approximately 2 μm and 4 μm offset lengths are realized. Figure 4(c) shows the transfer curves, in which the on-state current of the 2 μm offset HVTFT is one order larger than that of the 4 μm one. In the output curves (figure 4(d)), both devices show typical HVTFT performance with three distinguishable regions as in figure 2(g). However, the 2 μm offset device shows a smaller V_{kink} of 95 V, about 20 V smaller than that in the 4 μm one. This phenomenon is also found in other reports [5, 9, 14, 15, 19], and can be explained by the device physics simulation. The electric field is nearly constant in most of the offset region [9, 33, 34], which means that high electric field strength could be mitigated by longer offset region. The introduction of 4 μm offset region results in a reduced electric field of 0.49 MV cm^{-1} near the gate edge, which is about half of that in the 2 μm offset device as can be seen in figure 4(e). As a tradeoff, the on-state current is reduced due to the series resistance of the offset region. Therefore, the offset length should be carefully designed to delicately balance between V_{kink} and I_{ON}.

3.5. High-voltage inverters

To explore the application of the self-aligned photolithography technology in high-voltage logic circuits, HV inverters

are constructed with an HVTFT drive and an HVD load (figure 5(a)). Compared with other HV inverters which require off-chip resistors [5, 6, 10], this work employs the on-chip HVD as the load for better scaling down and integration. The *I*–*V* characteristics of the HVD shows a rectification ratio of ~10^6 and V_{BR} more than 110 V. Figure 5(c) shows the voltage-transfer characteristics of the HV inverter with V_{DD} ranging from 10 V to 80 V in 10 V step. Inset shows that the voltage gain is approximately 5. In addition, the HV inverter also allows low-voltage operation (figure 5(d)) down to 1 V. The transient response performance of the HV inverters is discussed in the supporting information, figure S3. The successful fabrication of HV inverters with the presented self-aligned photolithography technology demonstrates its feasibility in promising high-voltage circuits.

4. Conclusion

We have presented a self-aligned photolithography technology for the fabrication of fully-transparent HVTFTs, HVDs and HV inverters to improve their uniformity. Optical simulation of the photolithography process was performed to explain the principle of the proximity exposure method. The 170 μm thick substrate was proved to be better than the 500 μm substrate through simulations and experiments. Furthermore, by modulating the exposure dose, the offset length, and thus the electrical performance, were delicately controlled. Finally, HV inverters were constructed with an HVTFT drive and an on-chip HVD load. The successful fabrication of HVTFTs, HVDs and HV inverters demonstrates the feasibility and huge potential of the presented self-aligned photolithography technology.

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